IN THE CLAIMS

1. (original) A method for testing the design of an integrated circuit (system IC) comprising the steps of:

(a) designing the system IC to have a predetermined number and pattern for its chip I/O pads;

(b) designing a packaging module to fan-out the I/O of the system IC to an expanded pitch of packaging I/O pads having a correspondence to said chip I/O pads;

(c) partitioning circuitry of said system IC into a functional circuit;

(d) designing said functional circuit as a corresponding test IC, wherein said test IC I/O pads conform to one of a sub-set of the number and pattern of said chip I/O pads;

(e) attaching said test IC to said packaging module with conductive material;

(f) exercising said test IC by applying signals and power to inputs of said packaging module at packaging I/O pads corresponding to said sub-set of chip I/O pads; and

(g) collecting test data corresponding to said test IC.

2. (original) A method for testing the design of an integrated circuit (system IC) comprising the steps of:

(a) designing said system IC to have a predetermined number and pattern for its chip I/O pads;

(b) designing a packaging module to fan-out the chip I/O to an expanded pitch of packaging I/O pads having a correspondence to said chip I/O pads;

(c) partitioning functionality of said system IC into a plurality of individual functional circuits;

(d) designing said plurality of individual functional circuits as a corresponding plurality of test ICs, wherein each of the test ICs conforms to one of a plurality of sub-sets of chip I/O pads making up said number and pattern of said chip I/O pads;

(e) attaching said plurality of test ICs to said packaging module with conductive material;

(f) interconnecting an I/O of a first test IC of said plurality of test ICs to an I/O of a second test IC of said plurality of test ICs external to said packaging module;

(g) operating said plurality of test ICs by applying signals and power to selected ones of said packaging I/O pads corresponding to said plurality of sub-sets of said number and pattern of said chip I/O pads; and

(h) collecting test data corresponding to operating said plurality of test ICs.

3. (original) The method of claim 2 further comprising the steps of:

redesigning a first test IC of said plurality of test ICs generating a redesigned first test IC in response to said test data;

replacing a corresponding one of said plurality of tests chips with said redesigned first test IC; and

repeating steps (e)–(g).

4. (original) The method of claim 2 further comprising the step of:

redesigning said functionality of said system IC in response to said test data.

5. (original) The method of claim 2 further comprising the steps of:

coupling said system IC onto a PCB for a system designed to use said system IC; and

operating said system IC to emulate at least one function of said system.

6. (original) The method of claim 2 further comprising the step of:

testing said system IC in a test fixture designed for said system IC.

7. (original) A test module for a production system IC having a particular number and pattern of chip I/O pads, comprising:

a test IC corresponding to a sub-set of a total functionality of said system IC, said test IC having a test IC I/O configuration corresponding to a sub-set of said particular number and pattern of chip I/O pads;

a packaging module designed for said production system IC, having a packaging I/O number and pattern of packaging I/O pads for receiving said particular number and pattern of chip I/O pads;

couplings for electrically coupling said test IC I/O configuration to selected ones of said packaging I/O pads corresponding to said sub-set of said particular number and pattern of chip I/O pads; and

couplings for electrically coupling test signals to said selected ones of said packaging I/O pads corresponding to said sub-set of said particular number and pattern of chip I/O pads.

8. (original) A test module for a production system IC having a particular number and pattern of chip I/O pads, comprising:

a plurality of test ICs corresponding to a sub-set of a total functionality of said system IC, each of said plurality of test ICs having a test IC I/O configuration corresponding to an individual sub-set of said particular number and pattern of chip I/O pads;

a packaging module designed for said production system IC, having a number and pattern of packaging system IC pads for receiving said particular number and pattern of chip I/O pads, said packaging module having packaging I/O pads;

couplings for electrically coupling said test IC I/O configuration of each of said plurality of test ICs to selected ones of said packaging I/O pads corresponding to said sub-set of said particular number and pattern of chip I/O pads; and

couplings for electrically coupling test signals to said selected ones of said packaging I/O pads corresponding to said sub-set of said particular number and pattern of chip I/O pads.